160-190 GHz Monolithic Low Noise Amplifiers

Y. L. Kok, H. Wang, T. W. Huang, R. Lai, Y. C. Chen, M. Sholley, T. Block,
D. C. Streit, P. H. Liu, B. R. Allen, L. Samoska*, and T. Gaier*, Mike Barsky

TRW Space & Electronics Group
One Space Park, Redondo Beach, CA 90278, USA

*Jet Propulsion Laboratory
4800 Oak Grove Drive, Pasadena, CA 91109, USA

ABSTRACT

This paper presents the results of two 160-190 GHz monolithic low noise amplifiers (LNAs) fabricated with 0.07-μm pseudomorphic (PM) InAlAs/InGaAs/InP HEMT technology using a reactive ion etch (RIE) via hole process. A peak small signal gain of 9 dB was measured at 188 GHz for the first LNA with a 3-dB bandwidth from 164 to 192 GHz while the second LNA has achieved over 6-dB gain from 142 to 180 GHz. The same design (second LNA) was also fabricated with 0.08-μm gate and a wet etch process, showing a small signal gain of 6 dB with noise figure 6 dB. All the measurement results were obtained via on-wafer probing. The LNA noise measurement at 170 GHz is also the first attempt at this frequency.

INTRODUCTION

Millimeter-wave (MMW) LNA's are very important components for smart munitions, passive imaging and radiometer applications. The PM HEMT devices with both GaAs and InP materials have demonstrated high gain and low noise capability at W-band (75-110 GHz) and D-band (110-170 GHz) frequencies for hybrid integrated circuits [1]-[2]. High gain, low noise amplifiers have been successfully developed up to 160 GHz [3]-[6], [10]-[14]. For the frequency range above 120 GHz, InP-based HEMTs are superior to GaAs-based HEMT's for amplification due to the higher electron peak drift velocity in the InP based HEMT devices. The MMIC LNA's fabricated with the InP HEMT MMIC process have also achieved high gain and low noise figure performance at lower frequencies. Examples include a Q-band (44.5 GHz) two-stage balanced LNA exhibiting 2.2-dB noise figure (NF) with 20-dB associated gain [7], and a W-band four-stage balanced amplifier with a small signal gain of 23 dB from 75 to 110 GHz [8]. A two-stage cryogenically cooled W-band LNA also exhibited 0.7-dB NF at 95 GHz with 12-dB associated gain [9]. The motivation of this work is to demonstrate the feasibility of MMIC LNAs with better performance at higher frequency via the improvement of device and process technology.

This paper describes the design, fabrication, and testing of two 160-190 monolithic two-stage balanced amplifiers. Compared with the previously reported InP HEMT MMIC LNAs [5]-[9], [11], [14] fabricated with 0.1-μm InAlAs/InGaAs/InP PM HEMT technology, this work has the following new features in MMIC technology: (1) 0.07-μm gate-length HEMT for higher f_T

and fmax, (2) a reactive ion-etch (RIE) via hole process replacing the wet chemical etch for lower grounding inductance, and (3) a 2-mil InP substrate instead of 3 mil to maintain single mode propagation at high frequencies. All these are important to push the MMIC LNA performance at high frequencies to 180 GHz and higher. Regarding the measured performance of the two MMIC LNAs, a peak small signal gain of 9 dB was measured at 188 GHz for the first LNA with a 3-dB bandwidth from 164 to 192 GHz, while the second LNA has achieved over 6-dB gain from 142 to 180 GHz. All the measurement results were obtained via on-wafer probing. The encouraging results are due to the improved device and MMIC process technology, as well as the circuit design techniques for the high frequency.

DEVICE CHRACTERISTICS AND MMIC FABRICATION

The two 160-190 GHz MMIC LNA chips were fabricated on a 2-mil Fe-doped semi-insulating InP substrate grown by molecular beam epitaxy and employ 0.07-μm T-gate InP HEMT devices. The InAlAs/InGaAs/InP HEMT ($In_{0.65}Ga_{0.35}As$ channel) process follows the procedures reported in [2], with an additional wafer passivation and stabilization bake steps introduced to the MMIC process [11]. Figure 1 shows the InP HEMT device layer structure. The target device pinchoff voltage of -0.25 V with the voltage at a peak transconductance (Vgp) of 1000 mS/mm, are attained with a unity current gain frequency (fT) of 220 to 240 GHz, and a maximum oscillation frequency (fmax) of 500 GHz. For the MMIC process, precision NiCr resistors with a target resistance of 100 Ω/square and silicon nitride MIM capacitors with a target sheet capacitance of 300 pF/mm^2 are used. After processing the front side, the wafers are lapped and polished to 50 μm (2 mil) thickness. Ground via holes are etched using RIE technique and 3.5-μm gold is plated on the backside of the wafers to complete the MMIC process. Detailed information of the new MMIC process will be published elsewhere.

DEVICE MODELING AND CIRCUIT DESIGN

The linear small signal model for a 0.07-mm gate PM InP HEMT, used in the 160-190 GHz LNA design, was obtained from an estimation of the existing 0.1-mm gate HEMT equivalent circuit model [14] by scaling the critical model parameters such as Cgs, Cgd, Rds, and Rg, etc. Therefore there are some discrepancies between circuit simulation and measured results. The device model should be reinvestigated by measuring the device small signal S-parameters to high frequency.

Figure 2 shows the chip layouts photographs with the chip size of 2.4 mm x 1.7 mm and 2.6 mm x 1.7 mm. Both of the amplifiers have two stages with each stage being balanced design. Each stage uses the two gate-finger 30-μm PM InP HEMT device for low gate resistance and gate-drain capacitance to have high device gain at the desired frequency (160-190 GHz). This device has a maximum available gain of about 7.5 dB at 180 GHz. The circuits utilize a simple quasi-low-pass topology to minimize the uncertainties in the analysis and modeling at such a high frequency and thus reduce the design risk. Each amplifier uses four Lange couplers for the balanced design to improve the input/output return loss and the amplifier stability. The first one is designed for high gain at 180-190 GHz frequency range while the second one is targeted for a wider bandwidth from 150 to 180 GHz. The input and output matching networks are all constructed by cascading high-low impedance microstrip lines on a 50-μm thick InP substrate in

order to maintain single mode operation at high frequency. Metal-insulating-metal (MIM) capacitors are used for dc blocking and radial stubs are employed for RF bypass. Shunt RC networks are included in the bias circuitry to maintain amplifier stability. Reactive ion-etched via holes are used on 2-mil substrate so as to reduce the grounding inductance, as well as for better control of the etching area. All the passive structures were analyzed via full-wave electromagnetic (EM) analysis tool (SONNET software), as previously reported W-band design [10]. In particular, the Lange couplers have been carefully investigated to ensure the performance (3-dB and 90° phase shift) around 180 GHz.

AMPLIFIER MEASUREMENT

The 160-190 GHz MMIC LNAs were tested at a 140-220 GHz network analyzer via on-wafer probing. The block diagram of the measurement set up is shown in Fig. 3. To make the measurement, we input a swept frequency rf signal (with a frequency f_i between 11 and 18 GHz) into a multiplier, which multiplies the signal 12 times. The signal, now between 140 and 220 GHz, is fed into an attenuattor to prevent amplifier saturation, and then onto the DUT on-wafer, using D-band waveguide probes from GGB Industries. To down-convert the amplifier output, after the output probe, we used a harmonic mixer, driven by a local oscillator with $f_{LO}=f_i+20$ MHz. The amplifier output mixes with the LO to produce a 20 MHz IF, which is amplified and fed into the network analyzer. To calibrate out the system response, the amplifier signal is compared to an on-wafer thru-line, and the results are shown in the gain vs. frequency curves of Figure 4.

The small signal gain from 140 to 200 GHz of the first LNA is shown in Fig. 4(a). A peak small signal gain of 9 dB was measured at 188 GHz for the first LNA with a 3-dB bandwidth from 164 to 192 GHz. For the second LNA, Figure 4(b) plots the small signal gain from 140 to 200 GHz showing over 6-dB gain from 142 to 180 GHz. The dc bias for the first LNA and second LNA are Vd = 1.25~1.4 V with Id = 32.8 mA and Vd =1.3~1.41 V with Id = 42.8 mA. The dc power consumptions are 43.63 mW and 58.41 mW, respectively.

For comparison purposes, both of the amplifiers have been fabricated with a 0.08-mm gate-length HEMT and wet etch via hole MMIC process on an earlier wafer. On this previous wafer the first LNA achieved 7.2 dB gain at 190 GHz and over 5 dB from 170 to 194 GHz [15]. The second LNA had 5 dB over 152 to 180 GHz. Generally speaking, the amplifier performance from the new 0.07-μm gate with RIE via holes are 2-3 dB better than that from the earlier attempted process (0.08-μm gate with wet via holes) under a similar bias condition. The second LNA (using the 0.08-μm gate and wet via hole process) has been measured for noise at 170 GHz and demonstrated a noise figure of 6 dB with an associated gain of 6 dB, also via on-wafer probing. This is not only the first attempt of an on-wafer noise figure measurement of an LNA at this frequency, but also a significant noise performance of an LNA compared with the previously reported 155 GHz LNA noise figure results (5.1 dB NF with gain of about 4 dB per stage) [14]. More measurement and modeling results will be presented in the symposium.

SUMMARY

We have described the design and measurement results of two 160-180 GHz monolithic

low noise amplifier using 0.07-μm PM InGaAs/InAlAs/InP HEMT technology with dry-etched via holes. The first monolithic LNA designed for higher gain exhibits a small signal gain of 9 dB at 188 GHz, and more than 6 dB of gain from 164 to 192 GHz. The second LNA, designed for a wider bandwidth, has over 6 dB from 142 to 184 GHz. A same design of the second LNA but fabricated with 0.08-μm HEMT and wet etched via holes shows 6-dB gain and 6-dB NF at 170 GHz. These results define the state-of-the-art performance of highest frequency MMIC LNAs to date.

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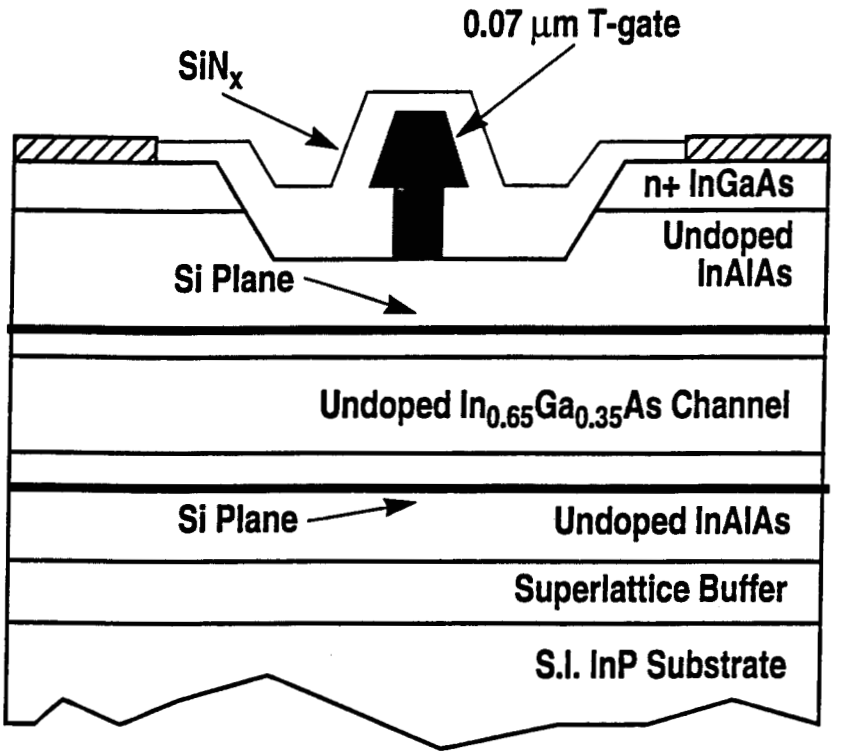
FIGURE CAPTIONS

Fig. 1. InGaAs/InAlAs/InP PM HEMT device layer structure.
Fig. 2. (a). Chip layout of the InP-based HENT LNA (ALH250C) with 9 dB gain peak at 168 and 188 GHz.
(b). Chip layout of the InP-based HEMT LNA (ALH252C) with gain greater than 6 dB from 142 to 180 GHz.
Fig. 3. Block diagram of the 140-220 GHz network analyzer test set.
Fig. 4. Measured small signal gain of (a) first, (b) second, MMIC LNA vs. frequency. The bias conditions are Vd = 1.25~1.4 V with Id = 32.8 mA for the first LNA and Vd = 1.31~1.41 V with Id = 42.8 mA for the second one.



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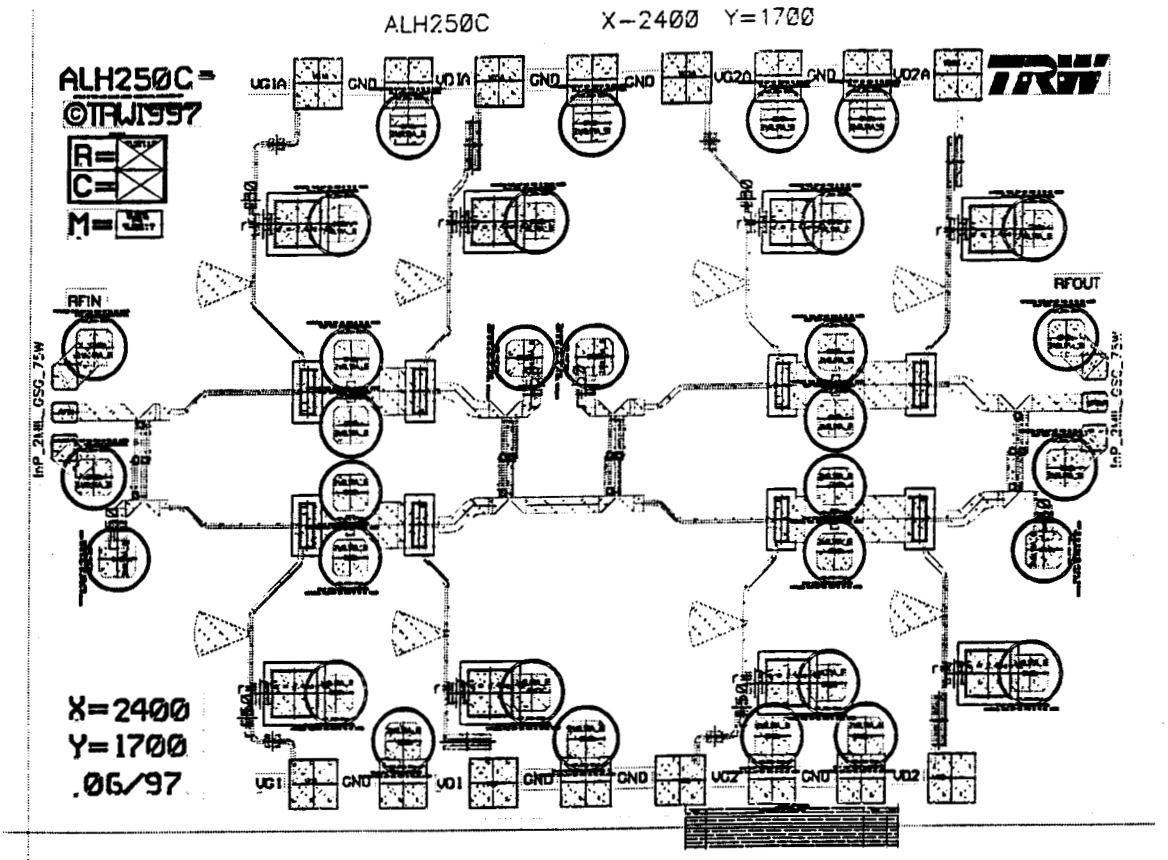


Fig. 2. (a). Chip layout of the InP-based HENT LNA (ALH250C) with 9 dB gain peak at 168 and 188 GHz.

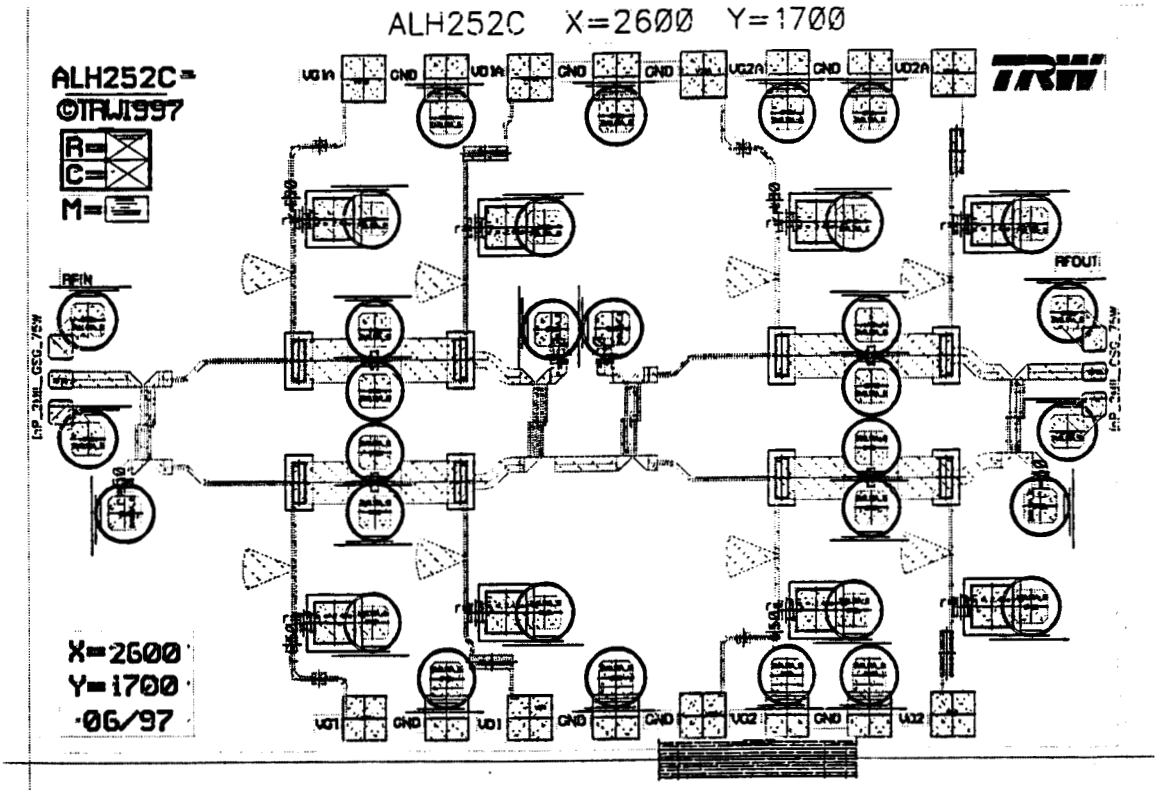
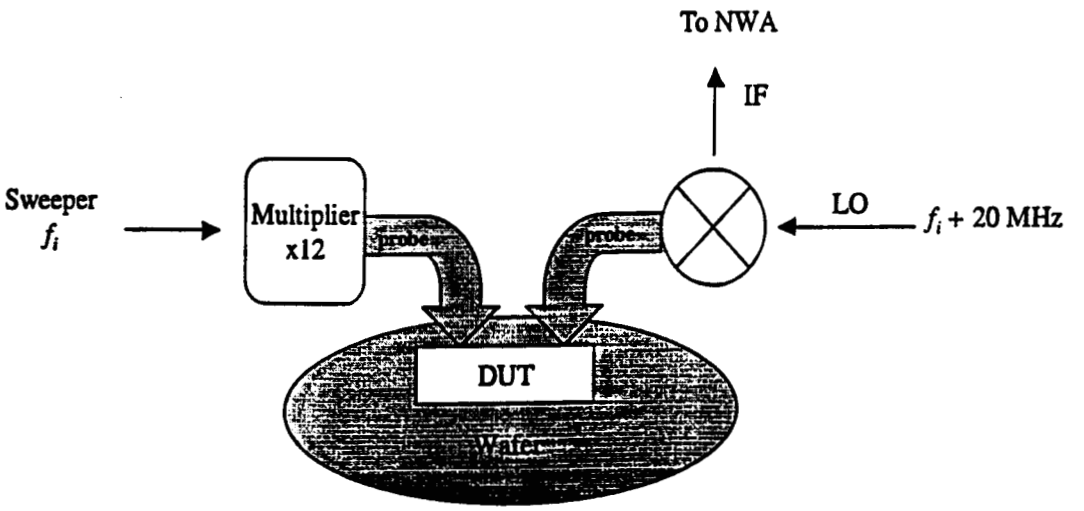


Figure 2(b). Chip layout of the InP-based HEMT LNA (ALH252C) with gain greater than 6 dB from 142 to 180 GHz.



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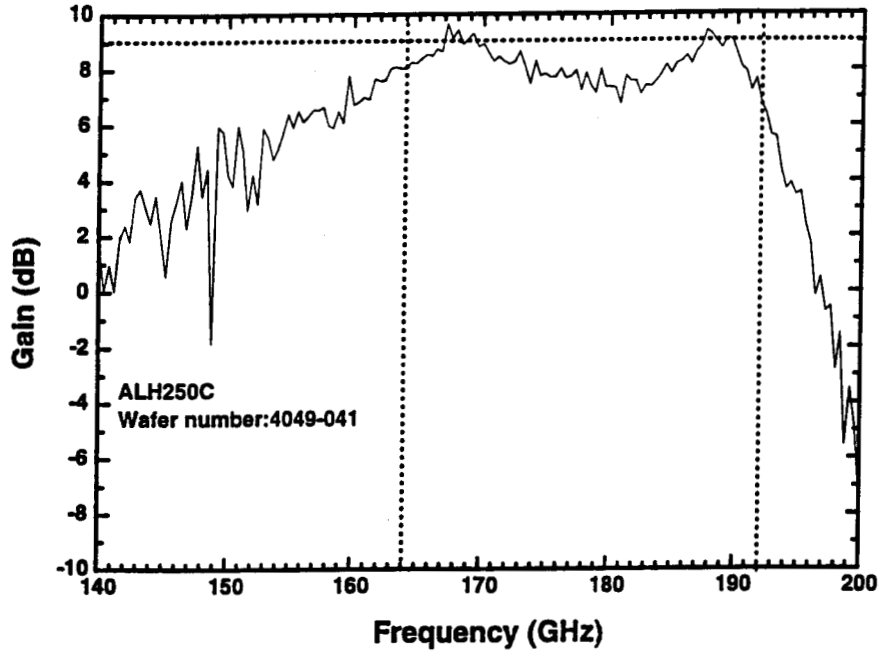
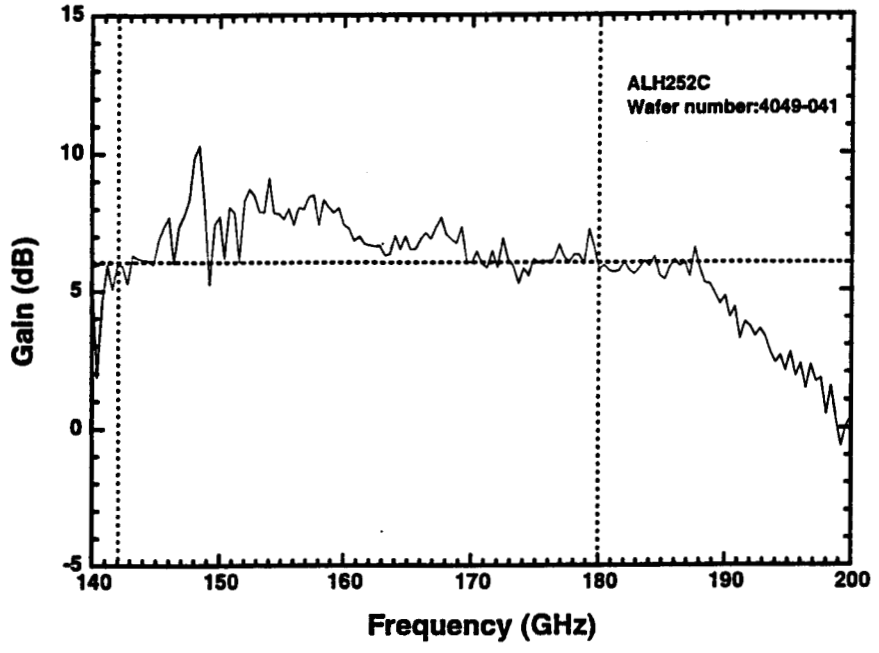


(a)



(b)

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